REMARKS

Claims 9-30 are pending in this application. By this Preliminary Amendment, claims 1-8 are cancelled, the specification is amended and new claims 9-30 are added. Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attachment is captioned " Version With Markings To Show Changes Made."

The specification is amended to incorporate specific reference to the two parent applications. The additional specification amendments correspond with amendments made in the parent Application No. 10/139,248.

An Information Disclosure Statement is also being filed together with Form(s) PTO-1449 listing references of record in the parent applications for the Examiner's initialing to make such art of record in the present application.

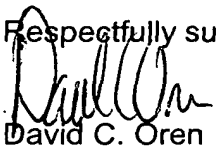
A Claim for Priority is also being filed. A certified copy of the Japanese priority documents were already filed in parent Application No. 09/149,666.

Applicants request a prompt examination (on the merits) for claims 9-30.

To the extent necessary, applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees and excess claim fees, to Deposit

Account No. 01-2135 (referencing case No. 500.36547CC3) and please credit any excess fees to such deposit account.

Respectfully submitted,



David C. Oren
Registration No. 38,694
ANTONELLI, TERRY, STOUT & KRAUS, LLP

DCO/pay
(703) 312-6600

Version With Markings To Show Changes Made

IN THE SPECIFICATION:

The paragraph beginning on page 7, line 13, has been amended as follows:

Fig. 1 illustrates a general configuration of the first embodiment. The system of the first embodiment is configured to have one or more processing units 100, one primary controller 104, one or more disk units 105 connected to the primary controller 104, one secondary controller 109, and one or more disk units 105 connected to the secondary controller 109. The processing unit 100 is composed of a CPU 101, a main storage 102, and a channel 103. The primary controller 104 contains a control memory 107 and a cache memory 108. The control memory 107 and the cache memory 108 are non-volatilized. For enhancing the reliability, each memory may be dualized. The cache memory 108 or the control memory 107 is composed of a semiconductor memory. As compared with the disk unit 105, the memory 107 or 108 provides a faster accessing capability by one or two digits. The primary controller 104 operates to transfer data between the processing unit 100 and the disk unit 105. Further, according to the present invention, the primary controller 104 provides a function of transferring data with the secondary controller 109. Or, the primary controller 104 contains one or more directors 106, each of which may operate to transfer data between the processing unit ~~200~~ 100 and the disk unit ~~205~~ 105 and between the secondary controller 109 and the director 106 itself. The internal arrangement of the secondary controller 109 is likewise to that of the primary controller 104.

The paragraph beginning on page 21, line 21, has been amended as follows:

In correspondence with the above, the control memory [109] 107 of the master secondary controller 700 stores a write time 701 of the secondary controller. This write time 701 is the information corresponding to the secondary controllers 109 containing the master secondary controller 700. The write time 701 of each secondary controller corresponds to the information periodically received by the master secondary controller 700 from each secondary controller 109 at the earliest time (the reference time on which the secondary controller 109 selects the secondary controller 109 in the second embodiment) among all the primary controller write enable times 500 contained in the secondary controller 109.

The paragraph beginning on page 25, line 18, has been amended as follows:

According to this embodiment, the master controller 700 is arranged to receive the information required for calculating the reference time from the secondary controller 109. In place, it may be arranged to receive the information from the primary controller 104 as shown in Fig. 7. In this case, the control memory 108 of the master secondary controller 700 stores a master primary controller write time 800. The write time 800 corresponds to the primary controller 104. The write time 800 is set as follows. The master secondary controller 700 receives the earliest write time 111 included in all the write data managing information 113 containing the necessity bits 124 being set at a proper period and sets it as the write time 800 inside of the primary controller ~~109~~ 107. For the master write time 702, the master secondary controller 700 operates to refer to

all the primary controller write times 701, select the earliest time and set it as the master write time 702 at a proper period. Like the foregoing embodiments, the reference time for the destaging or the data scrapping is the master write time 702.